CS 118
Midterm EXAM

1. Briefly define each of following:

   A. arithmetic and logic unit (ALU)
   B. chip
   C. computer architecture
   D. computer organization
   E. core
   F. deeply embedded system
   G. instruction set architecture (ISA)
   H. memory management unit (MMU)
   I. Amdahl's law
   J. cycles per instruction (CPI)
   K. instruction execution rate
   L. SPEC
   M. access time
   N. addressable unit
   O. cache memory
   P. memory hierarchy
   Q. transfer rate
2. What, in general terms, is the distinction between computer organization and computer architecture?
3. What are the four main functions of a computer?
4. Explain the concept of performance balance.
5. List the desirable characteristics of a benchmark program.
6. What are the SPEC benchmarks?
7. What types of transfers must a computer's interconnection structure (e.g., bus) support?
8. List and briefly define the PCIe protocol layers
9. What is the key distinguishing feature of a microprocessor?
10. For each of the following examples, determine whether this is an embedded system, explaining why or why not.
    a. Is the internal microprocessor controlling a disk drive an example of an embedded system?
    b. I/O drivers control hardware, so does the presence of an I/O driver imply that the computer executing the driver is embedded?
    c. Is a PDA (Personal Digital Assistant) an embedded system?
    d. Is the microprocessor controlling a cell phone an embedded system?
    e. Are the computers in a hardware-in-the-loop (HIL) simulator embedded?

11. How do data locality and instruction locality relate to spatial locality and temporal locality?

12. A processor accesses main memory with an average access time of T2. A smaller cache memory is interposed between the processor and main memory. The cache has a significantly faster access time of T1<T2. The cache holds, at any time, copies of some main memory words and is designed so that the words more likely to be accessed in the near future are in the cache. Assume that the probability that the next word accessed by the processor is in the cache is H, known as the hit ratio.
    a. For any single memory access, what is the theoretical speedup of accessing the word in the cache rather than in main memory?
    b. Let T be the average access time. Express T as a function of T1,T2, and H. What is the overall speedup as a function of H?
    c. In practice, a system may be designed so that the processor must first access the cache to determine if the word is in the cache and, if it is not, then access main memory, so that on a miss (opposite of a hit), memory access time is T1+T2. Express T as a function of T1,T2, and H. Now calculate the speedup and compare to the result produced in part (b).

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13. Four benchmark programs are executed on three computers with the following results:

	Computer A	Computer B	Computer C
Program 1	1	10	20
Program 2	1000	100	20
Program 3	500	1000	50
Program 4	100	800	100

The table shows the execution time in seconds, with 100,000,000 instructions executed in each of the four programs. Calculate the MIPS values for each computer for each program. Then calculate the arithmetic and harmonic means assuming equal weights for the four programs, and rank the computers based on arithmetic mean and harmonic mean

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18. A microprocessor has an increment memory direct instruction, which adds 1 to the value in a memory location. The instruction has five stages: fetch opcode (four bus clock cycles), fetch operand address (three cycles), fetch operand (three cycles), add 1 to operand (three cycles), and store operand (three cycles).
    a. By what amount (in percent) will the duration of the instruction increase if we have to insert two bus wait states in each memory read and memory write operation?
    b. Repeat assuming that the increment operation takes 13 cycles instead of 3 cycles

19. Consider a 32-bit microprocessor, with a 16-bit external data bus, driven by an 8-MHz input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals four input clock cycles. What is the maximum data transfer rate across the bus that this microprocessor can sustain, in bytes/sec? To increase its performance, would it be better to make its external data bus 32 bits or to double the external clock frequency supplied to the microprocessor? State any other assumptions you make, and explain. *Hint:* Determine the number of bytes that can be transferred per bus cycle.

20. Consider two microprocessors having 8- and 16-bit-wide external data buses, respectively. The two processors are identical otherwise and their bus cycles take just as long.
    a. Suppose all instructions and operands are two bytes long. By what factor do the maximum data transfer rates differ?
    b. Repeat assuming that half of the operands and instructions are one byte long.

22. A computer has a cache, main memory, and a disk used for virtual memory. If a referenced word is in the cache, 20 ns are required to access it. If it is in main memory but not in the cache, 60 ns are needed to load it into the cache, and then the reference is started again. If the word is not in main memory, 12 ns are required to fetch the word from the disk, followed by 60 ns to copy it to the cache, and then the reference is started again. The cache hit ratio is 0.9 and the main memory hit ratio is 0.6. What is the average time in nanoseconds required to access a referenced word on this system?
23. 4.9 Assume a processor having a memory cycle time of 300 ns and an instruction processing rate of 1 MIPS. On average, each instruction requires one bus memory cycle for instruction fetch and one for the operand it involves.
    a. Calculate the utilization of the bus by the processor.
    b. Suppose that the processor is equipped with an instruction cache and the associated hit ratio is 0.5. Determine the impact on bus utilization.
24. 5.14 Describe a simple technique for implementing an LRU replacement algorithm in a four-way set-associative cache

25. Convert the following binary numbers to their decimal equivalent.
    a. a) 1000111
    b. b) 10110101
    c. c) 11111100

Give the binary two's complement representation of the following decimal numbers.

a) -56
b) b) -111

A vehicle can be started only when the following conditions are satisfied. • the brake is ON. • the gearbox is in NEUTRAL. • The seat belt is ENGAGED.

(a) What single logic device can be used to accomplish this, and construct the truth table for this circuit.

(b) If only two input NAND gates are available, draw the logic diagram with the outputs of each gate clearly identified.

26. Write the truth table for each of the gate circuits shown below.

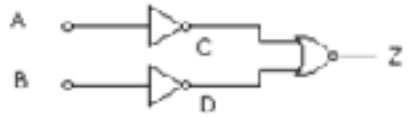


Figure 3.6.1

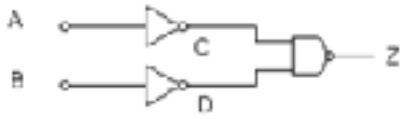


Figure 3.6.2

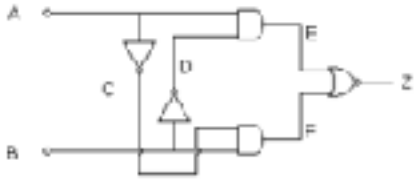


Figure 3.6.3

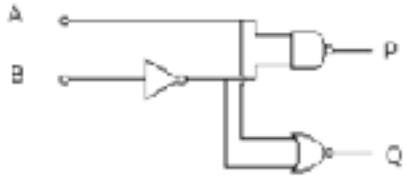


Figure 3.6.4